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A low complexity joint equalizer and decoder for 1000Base-T Gigabit Ethernet

Haratsch, E.F. Azadet, K.

DSP & VLSI Syst. Res., Lucent Technol. Bell Labs., Holmdel, NJ, USA;

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Abstract

A VLSI architecture for low complexity joint decoding and equalization for 1000Base-T Gigabit Ethernet is presented. A one-tap parallel decision-feedback decoder jointly decodes the trellis and cancels the first tap of the post-cursor channel impulse response. The one-dimensional branch metrics are precomputed in a look-ahead fashion to meet the speed requirements. The less significant tail of the impulse response is canceled with a simple decision-feedback prefilter. The design has been implemented in 0.25 μm standard cell CMOS process for operation at 125 MHz.

Index Terms

Inspe

Controlled Indexing

CMOS digital integrated circuits VLSI application specific integrated circuits decision feedback equalizers decoding digital signal processing chips high-speed integrated circuits interference suppression intersymbol interference local area networks trellis coded modulation

Non-controlled Indexing

0.25 micron 1000Base-T Gigabit Ethernet 125 MHz 3.3 V ISI cancellation TCM signal VLSI architecture decision-feedback prefilter decoding equalization low complexity joint equalizer/decoder one-dimensional branch metrics one-tap parallel decision-feedback decoder post-cursor channel impulse response standard cell CMOS process trellis code

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References

No references available on IEEE Xplore.

Citing Documents

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